Notice of Allowability	Application No.	Applicant(s)	
	09/699,077	ISHIDA ET AL.	
	Examiner	Art Unit	
	Ayal I. Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *After Final Amendment filed 3/24/05*.

2. ☒ The allowed claim(s) is/are *1,5,7-9 and 13-16*.

3. ☒ The drawings filed on *27 October 2000* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Introduction

1. Claims 1, 5, 7-9, and 13-16 of U.S. Application 09/699,077, originally filed on 10/27/2000 are presented for examination. The application claims Foreign Priority to Japanese Application 14962/00, filed on 1/24/2000.
2. The Examiner indicated in the Final Office Action (dated 11/3/2004) that dependent claims 3, 5, and 7 were allowable.
3. The Applicants, in their After Final Amendment (dated 3/24/2005), have rolled up claim 3 and intermediate claim 2 into independent claim 1.
4. Claim 5 has been rewritten into independent form by including the limitations of intermediate claim 4 and independent claim 1.
5. Claim 7 has been rewritten into independent form by including the limitations of intermediate claim 6 and independent claim 1.
6. Claims 8-9 depend from claim 1, claims 13-14 depend from claim 5, and claims 15-16 depend from claim 7.
7. The application is now in condition for allowance. The following paragraphs provide the detailed reasons for allowance.

EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

8. The following is an Examiner's statement of reasons for the indication of allowable subject matter.

9. The closest prior art of record is:

   a. Cole, Jr. et al. U.S. Patent 6,031,386. (Henceforth referred to as "**Cole**").

   b. Acuna, E.L. et al. "Simulation Techniques for Mixed Analog / Digital Circuits." IEEE Journal of Solid-State Circuits. Vol.25, Issue 2. pp.353-363. (Henceforth referred to as "**Acuna**").

10. In regards to Claim 1, Cole teaches the following limitations of Claim 1 (emphasis added):

> 1. A fault simulation method for a semiconductor IC, said method comprising the steps of:
>
> generating a test pattern sequence composed of two or more test patterns for input to said semiconductor IC;

Cole teaches "[a] means connected to a plurality of input pins or terminals of the IC for providing a vector set of voltage inputs to the IC for toggling the IC between logic states thereof." (Cole, especially: col.2, line 65 to col.3, line 5).

Cole also teaches "The means for providing the vector set of voltage inputs to the IC can comprise a switch matrix, or preferably an integrated circuit tester." (See Cole, col.3, lines 17-20). Examiner interprets Applicants' "test pattern sequence" as corresponding to Cole's "vector set of voltages".

> **performing a logic simulation** of the operation of said semiconductor IC in the case of applying thereto each of said two or more test patterns of said test pattern sequence, and calculating a logic signal value sequence in each signal line in said semiconductor IC; and

Cole teaches "... and identifying ICs having defects or failure mechanisms therein by determining whether the transient voltage component V_{DDT} exceeds a known value. The known value can be derived from measurements of one or more defect-free ICs using the present invention, or derived from numerical

modeling of electrical characteristics of the IC (i.e. from modeling of a design for the IC)." (See Cole, especially: col.3, lines 40-46).

> **generating a list of faults for each logic gate in said semiconductor IC**, which are detectable by **a transient power supply current testing** using said test pattern sequence, through the use of said logic signal value sequence in said each signal line calculated by said logic simulation.

Cole teaches "toggling the IC between logic states by providing a vector set of voltage inputs to input pins of the IC ... and identifying ICs having defects or failure mechanisms therein by determining whether the transient voltage component, V_{DDT} exceeds a known value. (Cole, especially: col.3, lines 35-46).

Examiner notes that Cole teaches two embodiments of his invention: 1) measuring a transient voltage component V_{DDT} (col.3, lines 32-46) and 2) measuring a time delay in a transient voltage component V_{DDT} (col.3, lines 48-62). In both embodiments, the measured values are compared to "known values" derived from numerical modeling of the IC.

Moreover, Cole also teaches (see col.3, lines 35-46) "... toggling the IC between logic states by providing a vector set of voltage inputs to input pins of the IC ... and identifying ICs having defects or failure mechanisms therein by determining whether the transient voltage component, V_{DDT} exceeds a known value." Examiner interprets that the list of "defects or failed mechanism" constitutes a "fault list".

However, while Cole teaches a "transition simulation", it does not expressly teach a "logic simulation" as claimed. (See Applicants' arguments in the amendment dated 2/19/04, p.7.) As argued by the Applicants, the difference

between the two types of simulation as follows: "A transition simulation must account for the timing of signal transitions ...", while "A logic simulation does not need to account for the timing of signal transitions. It considers state logic levels." Examiner has interpreted the term "logic simulation" in light of Applicants' arguments.

Moreover, Cole also does not expressly teach that the list of logic faults is created "for each logic gate in said semiconductor IC."

Acuna, on the other hand, teaches a simulator which performs four types of circuit simulation (see Acuna, Section II, pp.354-355): 1) Electrical Analysis, 2) Logic Analysis, 3) Electrical-Logical (ELOGIC) Analysis, and 4) Time Step Synchronization. Examiner interprets that the ELOGIC Analysis corresponds to the claimed "logic simulation."

Acuna also teaches (see Section "II.B Logic Analysis") that "Inertial delay models are used for all gates except for the pass transistor. The delay can be specified as fixed values or fan-out-dependent values which depend on the output capacitive loading."

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Cole with those of Acuna, because Acuna teaches the use of both analog and digital simulation of mixed analog/digital MOS circuits (see Acuna, Abstract), which is what is needed to simulate the MOS circuits in Cole's "numerical modeling" step (see Cole, col.3, lines 42-46).

11. On the other hand, neither Cole nor Acuna, either individually or in combination, teach the following limitations in combination with the other limitations of the claim:

> ... wherein said fault list generating step is a step of checking, for said each logic gate, whether a logic signal value sequence in an output signal line of said each logic gate has been changed, and if so, **generating said fault list in which an identifier of a test pattern sequence having changed said logic signal value sequence and said logic gate are registered in correspondence with each other**.

In particular, neither Cole nor Acuna expressly teach the generating the fault list in which "an identifier of a test pattern sequence having changed said logic signal value sequence" and "said logic gate" are registered in correspondence with each other.

12. Independent claims 5 and 7, which claim the same limitations, are allowed for the same reasons. All dependent claims are allowed for this reason.

Conclusion

13. Examiner notes that the closest related art consists of issued patents that were authored by the inventors of the instant application. Moreover, these references cannot be applied as prior art due to their filing dates, which post-date the filing date of the instant application. These patents are:

    a. U.S. Patent 6,828,815 (See Fig.18 and associated text)

    b. U.S. Patent 6,801,049 (See Fig.18 and associated text)

    c. U.S. Patent 6,593,765

    d. U.S. Patent 6,461,882 (See Fig.15 and associated text).

14. These references have been cited on the PTO-892 form.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749.

Any response to this office action should be faxed to (703) 872-9306, or mailed to:

USPTO
P.O. Box 1450
Alexandria, VA 22313-1450

or hand carried to:

USPTO
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon

Art Unit 2123

June 29, 2005

Paul L. Rodriguez 7/1/05

Primary Examiner
Art Unit 2125